WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor apparatus device including a plurality of layers on a semiconductor substrate, said method comprising the steps of:

dividing a pattern of at least a layer into a plurality of sub-patterns; and

joining the divided sub-patterns to perform patterning,

wherein as to a layer including wiring substantially affecting operation of the semiconductor device depending on a positional relationship to any other wiring, the patterning is performed by one-shot exposure using a single mask.

2. The method according to claim 1, wherein as to a layer including wiring in which a value of parasitic capacitance generated depending on the positional relationship to any other wiring substantially affects the operation of the semiconductor device, the patterning is performed by one-shot exposure using a single mask.

3. The method according to claim 2, wherein the semiconductor device has a plurality of elements each having a same structure composed of a plurality of layers including a plurality of a same

patterns respectively, and

as to a layer including wiring which causes dispersion of a characteristic of each of said elements, the dispersion substantially affecting the operation of the semiconductor device, when there are differences in the value of the parasitic capacitance among the elements, the one-shot exposure using a single mask is performed.

4. The method according to claim 3, wherein

the semiconductor device further has pixels each including a photoelectric conversion portion, and

as to a layer including wiring which causes an output difference of photoelectric conversion at a degree of being visible in an image, when there are differences in the value of the parasitic capacitance among the pixels, the one-shot exposure using a single mask is performed.

5. The method according to claim 4, the method further comprising the step of forming each of the pixels and/or a peripheral circuit by means of a CMOS process,

wherein control wiring of a field effect transistor in the pixel is formed by the one-shot exposure using a single mask.

6. The method according to claim 1, wherein wiring directly connected to the semiconductor substrate is formed by the one-shot exposure using a single mask.

7. The method according to claim 6, wherein the wiring is made of polysilicon.

8. The method according to claim 1, wherein only as to the layer including the wiring substantially affecting the operation of the semiconductor device depending on the positional relationship to any other wiring, the patterning is performed by one-shot exposure, and as to all of the other layers, the patterning is performed by division exposure.

9. The method according to claim 1, wherein as to layers to be patterned prior to the patterning of the layer including the wiring substantially affecting the operation of the semiconductor device depending on positional relationship to any other wiring, the patterning is performed by one-shot exposure, and as to all of the other layers to be patterned after the one-shot exposure, the patterning is performed by division exposure.

10. A method for manufacturing a semiconductor apparatus device, said method including the steps of dividing a pattern of at least one layer into a plurality of sub-patterns, and joining the divided sub-patterns to perform patterning, said method comprising the steps of:

forming source and drain regions of a MOS transistor on a semiconductor substrate;

forming a gate insulating film and a gate electrode of the MOS transistor;

forming a wiring layer including gate wiring connected to the gate electrode; and

forming the gate wiring by performing patterning by means of a one-shot exposure to the wiring layer.

11. The method according to claim 10, said method further comprising the step of forming a photoelectric conversion portion.